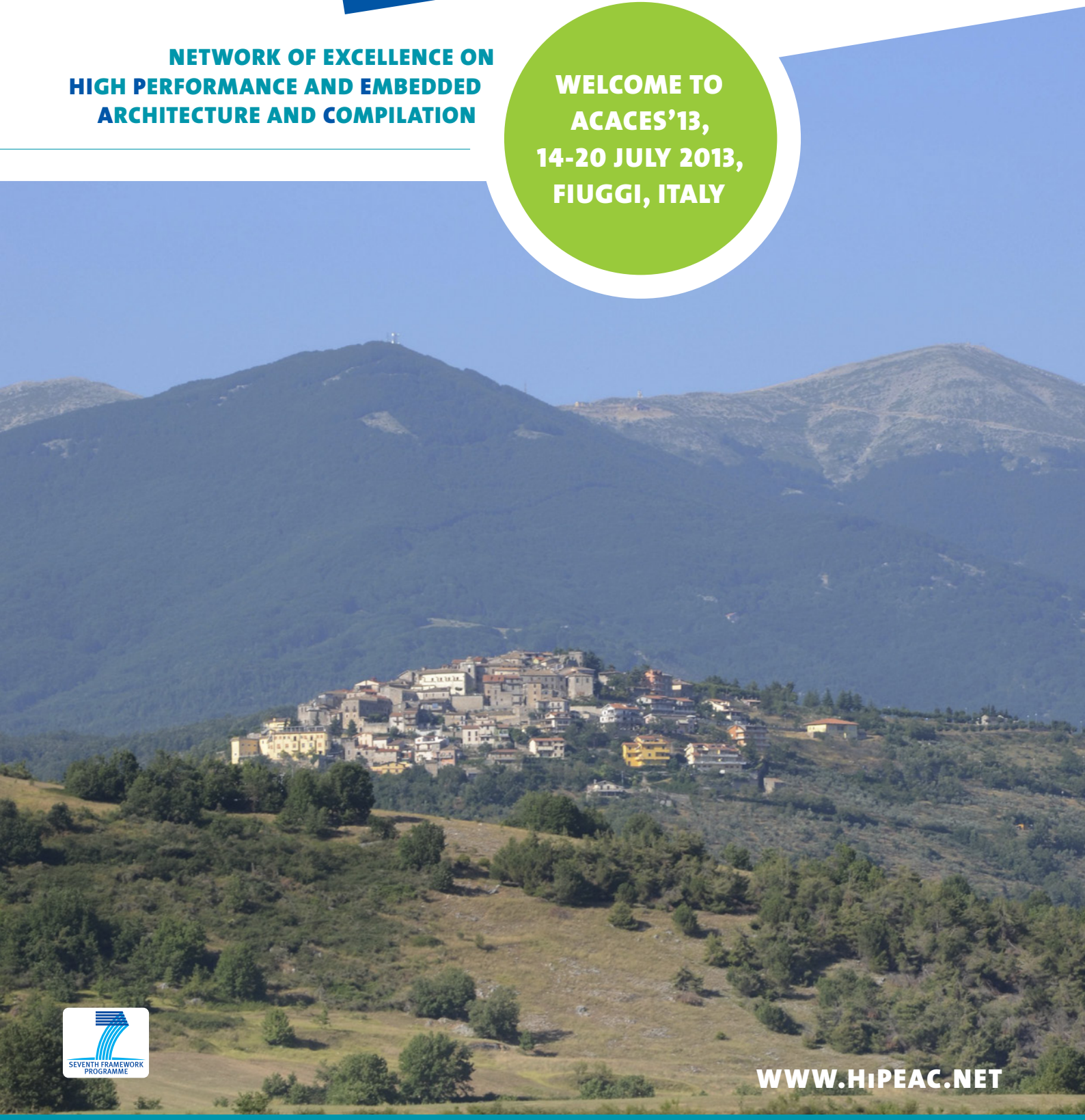
HiPEAC info 35

COMPILATION ARCHITECTURE

APPEARS QUARTERLY
JULY 2013

NETWORK OF EXCELLENCE ON
HIGH PERFORMANCE AND EMBEDDED
ARCHITECTURE AND COMPILATION

WELCOME TO ACACES'13, 14-20 JULY 2013, FIUGGI, ITALY



SEVENTH FRAMEWORK PROGRAMME

WWW.HIPEAC.NET

AUTUMN COMPUTING SYSTEMS WEEK, 7-9 OCTOBER 2013, TALLINN, ESTONIA

MESSAGE FROM THE HIPEAC COORDINATOR

Recently, I was struck by an article by Moshe Vardi, Editor-in-Chief of the Communications of the ACM who wrote that by 2045, artificially intelligent machines maybe capable of "if not any work that humans can do, then, at least, a very significant fraction of the work that humans can do". Recent signs of it are IBM Watson beating Jeopardy champions and now being trained as an oncologist and call center customer service manager, as well as self-driving cars and trucks, and automatic simultaneous translation. All these applications require advanced interpretation of lots of data, have been made possible by recent advances in artificial intelligence, and are fueled by powerful computing systems. These technologies will revolutionize the way we study, work, relax... They also lead to fundamental questions like: if computers do all the work, what will humans do? And, for higher education: which skills and competences should we teach to the next generation to prepare them for this future?

Last month, we learned that that the HiPEAC project officer Dr. Panos Tsarchopoulos has left the unit for Complex Systems and Advanced Computing for a new job in the unit for Future & Emerging Technologies (FET). He has been the project officer of HiPEAC since 2007, and in that role he always supported our community and encouraged us to raise the bar, and to aim for the next level. As the coordinator of HiPEAC, I am very grateful for all the support we got from him during those years. He contributed a lot to the success of the network. The new HiPEAC project officer is Dr. Max Lemke, who is also deputy head of the unit, and with whom we have already been collaborating intensively in the last couple of years. I am looking forward to working with him on the future of our community.

In April, we passed the first review of HiPEAC3. The reviewers congratulated the network on the results of the first year of HiPEAC3, in particular the increased impact of the HiPEAC conference in our community, the innovative journal-first publication model, the increased number of paper and technology transfer awards, the quality of the HiPEAC roadmap, and several other activities ... They encouraged HiPEAC to look for ways to further increase the impact of the network.

In May, we enjoyed the Spring Computing Systems Week in Paris, co-organized with ACM Europe. With 133 attendees, this was a well-attended networking event which allowed us to strengthen the links with ACM Europe. The next Computing Systems Week will take place in Tallinn, Estonia on October 7-9, 2013. On the Tuesday, it will feature a HiPEAC industry partner event.

This newsletter issue is the summer school issue. The summer school also marks the beginning of the summer break for me. I wish you a relaxing summer with your family and friends, and I hope to see you again after the summer holiday in good health, and full of plans for the year to come.

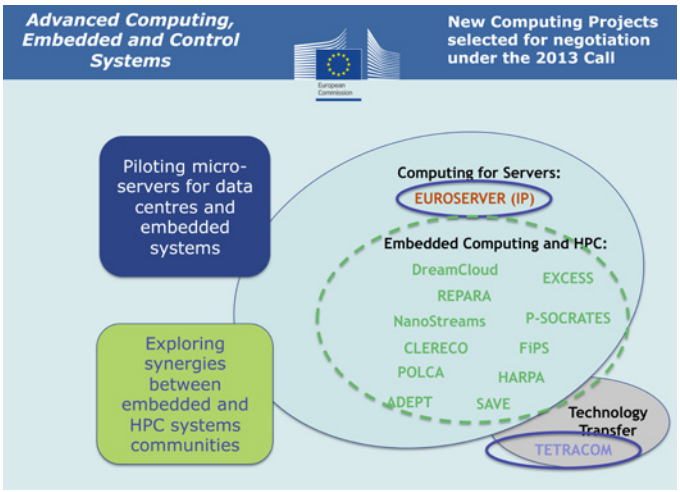
Take care,
Koen De Bosschere

CONTENT

MESSAGE FROM THE PROJECT OFFICER

Dear Colleagues,

Under the last Work Programme of Framework Programme 7, the European Commission is launching a significant number of projects in the area of Computing Systems:
Under "advanced embedded, computing, and control systems", one Integrated Project will pilot the concept of cost- and energy efficient micro-servers targeting data centres as well as embedded applications. Bringing together partners from both communities, 11 research projects will explore synergies between HPC and embedded systems. One technology transfer project will stimulate the adoption of novel computing technologies by industry. A total of around 40M€ European Commission contribution is planned to go to the area. More information about these projects will be available after summer.



On 1 July 2013, the Commission has launched the I4MS initiative - ICT for Manufacturing SMEs (77M€ Commission contribution). Through it, we want to connect innovators across value chains in manufacturing and engineering to better profit from newest advances in ICT. For users, that means reducing their risk in being an early adopter of innovative ICT. For suppliers, that means helping them to advance innovative prototypes towards a successful product. More than 35% of the initiative is related to computing:

To make the I4MS concept less abstract, let me give an example: Modelling and simulation technologies are established tools in large companies in manufacturing and engineering, often provided by world-leading companies from Europe including many SMEs. Large companies, like the automotive and aerospace manufacturers and their suppliers, have their own HPC (High Performance Computing) resources dedicated to simulation applications. SME users in small manufacturing businesses scattered across Europe until now were often not able to exploit these technologies for optimising the design and production of their products, because they could not get affordable access to tools, expertise, and computing resources. This is where the three of the seven I4MS projects FORTISSIMO, CloudSME and CloudFlow step in. The primary goal of about 80 cloud-based simulation experiments carried out by these projects is to pilot affordable one-stop pay-per-use simulation services for SMEs, which include Cloud-based HPC resources. Value chains in experiments typically include users, tool- and HPC resource providers, as well as experts. Projects and their experiments are implemented with the help of pan-European networks of competence centres, providing the knowledge and support for partnering across value chains and beyond national and regional borders.

In total about 110 SMEs are envisaged to take part in the cloud-based simulation projects of I4MS with more than 80 innovation experiments over the next 3 years. Only less than half of the experiments have been defined at the time of launch. There is plenty of opportunity for interested companies to apply for being part of the action. This can be done through responding to open Calls issued by projects starting from end of this year.

The I4MS initiative is a first pilot for wider integration of research and innovation under Horizon 2020. It is part of the Public Private Partnership 'Factories of the Future' (PPP FoF) launched in November 2008 within the European Economic Recovery Plan to respond to the global economic crisis.

Last not least, we are working on the first work programme for Horizon 2020. We hope to be able to say more in the next HIPEAC newsletter.

Max Lemke

Dear Colleagues,
Time has come for a new Project Officer to be responsible for HiPEAC. I would like to thank all and each one of you for the numerous exciting discussions and ideas that we have shared over the last years. I have appreciated your passion and enthusiasm for your work and for the development of cutting-edge computing research in Europe. It has been a real privilege for me to be the Project Officer of HiPEAC and I am sure that I will have the opportunity to meet many of you again in the future.

Panos Tsarchopoulos

HIPEAC SPRING COMPUTING SYSTEMS WEEK, PARIS

Thematic sessions in Paris, a new opportunity for discussing research challenges in the HiPEAC community

The Spring 2013 Computing Systems Week (CSW) of HiPEAC was held within the First ACM European Computing Research Congress (ACM ECRC) at the Palais des Congrès de Paris, on May 2-3, 2013. The goal of the ACM ECRC is to co–locate multiple (ACM) European research conferences, workshops, and/or research meetings to create a significant gathering of European computing researchers. Plenary sessions that addressed important issues in European computing research and receptions that fostered networking among European researchers contributed to make ACM ECRC a very well attended a successful event.

The program for the last Computing Systems Week in Paris was designed around seven thematic sessions, which resulted from a call launched in mid January. Before presenting a short summary of each one of the sessions and main conclusions, I just want to thank the organizers for the enthusiasm in preparing them and for their contributions to this summary in the HiPEAC Newsletter. Additional details about the presentations and slides for most of them are available through the HiPEAC website.

DYNAMIC COMPILATION

This thematic session brought together researchers engaged in various forms of Dynamic Compilation, from load-time code generation to runtime feedback-directed recompilation, from specific application domains to general-purpose applications. The goal was to facilitate knowledge sharing from this broad range of usage scenarios and compilation techniques, and through that to gain a better understanding of the range of problems that dynamic compilation is capable of addressing. In addition, the session analysed whether dynamic compilation is successfully applicable to other programming languages and application domains than those it was traditionally aimed at, and how far it is from addressing the challenges of today's computing world, including especially the ability of the computing environment to change at runtime.

The session included five presentations from academia (U. of Amsterdam, U. of Saarland, two from U. of Edinburgh and U. of Manchester) and three from industry (IBM, CEA and ST). The majority of the talks dealt with statically compiled languages, which confirms the growing relevance of dynamic optimizations to languages and scenarios other than those traditionally aimed at by JIT compilers. The ability of dynamic optimizers to address today's virtualized, dynamically changing environments, was less explored by the research works presented at this session, and is still an open question.

INTERMEDIATE REPRESENTATIONS

This thematic session on Intermediate Representations featured five talks that covered a broad range of innovative results and positions, all focusing on this core component at the heart of the compilation process. Starting with multiple position statements collected from a set of experts, Fabrice Rastello interactively interviewed each colleague who helped flesh out contradicting requirements from intermediate representations and the trade-offs involved. Perhaps one outcome of which is that a compromise to have multiple IR's may be inevitable. Roland Leißa then described an IR for AnyDSL, which supports efficient translation of higher-order functions as it is designed to support efficient code-generation via lambda lifting and dropping. It would be interesting to see if AIR indeed facilitates wider, more efficient and easier-to-use DSL's.

Boaz Ouriel presented a new Standard Portable IR, initiating a trilogy on three (related only by name) IR's named SPIR, SPIRE and INSPIRE. SPIR aims to extend the portability of OpenCL by providing a common binary/bitcode representation based on the widely used LLVM-IR. This standard representation should also provide new opportunities to connect other languages such as C++ AMP to heterogeneous platforms supporting OpenCL. Dounia Khaldi talked about SPIRE, providing a Sequential to Parallel IR Extension methodology. Reasoning about how to introduce parallel execution aspects into an IR, which is typically single-threaded, SPIRE employs ten new concepts that deal with the execution, synchronization and data distribution of a program, which are precisely defined via a formal semantics and rewriting rules. Finally, Herbert Jordan gave a closing talk about the high-level IR of the Insieme compiler project - INSPIRE, which provides a minimalized representation capable of capturing a diverse set of parallel languages including MPI, OpenMP, OpenCL, in a uniform manner. This provides a canonical basis for research of subsequent analysis and transformations such as auto-tuning mechanisms, applicable to a wide range of source programs and languages as desired. INSPIRE facilitates another intriguing line of research – that of processing and optimizing code written in a mix of several such languages.

THREAD-LEVEL SPECULATION

This session on Thread-Level Speculation (TLS) addressed several new and challenging techniques, allying advanced parallelisation transformations and time-overhead minimization, needed to take advantage of the inherent parallelism in programs that cannot be detected at compile-time or just by some previous dynamic analysis. The session started with two presentations on pretty advanced frameworks: Clemens Hammacher presented some interesting experiences in integrating Software Transactional Memory systems (STM) inside the Sambamba framework, and then a TLS conflict detection system at memory page

ACM President Vint Cerf during his keynote speech at ECRC in Paris.

Lunch banquet at the CSW in Paris

granularity. Benoît Pradelle presented the VMAD framework, which implements a speculative and dynamic adaptation of the polytope model. Then the session went on with two short presentations of some work in progress. Cédric Bastoul presented a technique allowing switching loop nests between different schedules at runtime. Emmanuel Riou and Nabil Hallou presented a currently developed tool called Padrone, which is dedicated to on-the-fly dynamic binary modifications.

The session continued with two additional presentations on work at the margin. Lawrence Rauchwerger presented a fully automatic and hybrid approach to loop parallelization that integrates the use of static and run-time analysis. It overcomes many known difficulties such as nonlinear, indirect array indexing and complex control flow. The framework validates the parallelization transformation by verifying the independence of the loop's memory references. Henri-Pierre Charles presented a hardware unit dedicated to generate code adapted to some target architecture and execution context, currently targeting on-the-fly GPU code generation.

HYBRID PROGRAMMING MODELS AND OPTIMIZATIONS FOR HETEROGENEOUS MANY-CORES

The thematic session on Programming Models and Runtime Systems focused on the alternatives for programming heterogeneous systems, incorporating accelerators, GPUs and/or FPGAs. It covered the topics from how to characterize and schedule the resources exposed by the hardware in the best way, how to exploit the differences and improve energy-savings, from mobile current and future platforms (Ben Gaster, keynote from Qualcomm) to high performance platforms; and from already existing languages to new directives and mixed programming languages (François Bodin, CAPS Enterprise and Samuel Thibault, Univ. of Bordeaux 1 and INRIA). The second part of the session consisted of a very active participation from current industry and university research results, including presentations from the PEPPHER and ENCORE projects. Questions about representative benchmarks, model limitations on OpenCL, task partition decisions, tuning block sizes, or most-suitable device to work with, were some of the questions in the interesting debate.

COMING CHALLENGES FOR THE INTERCONNECT

The main purpose of this thematic session on interconnection networks was to discuss the future challenges and problems that are emerging in this domain. Invited presenters were selected from a set of representative European companies leading different key initiatives. Cyriel Minkenberg and Mitch Gusat from IBM Zurich and John Taylor from Gnodal focused on off-chip interconnects; Gilles Baillieu from Arteris, Duco van Amstel from Kalray, and Marcello Coppola from ST Microelectronics focused on-chip interconnects. This last set of presentations was complemented with a presentation from academia (José Flich from Technical University of Valencia and Davide Bertozzi from University of Ferrara). The session was well attended, gathering key people in Europe working on industrial interconnect design across different application domains (high performance computing, embedded systems), fostering a productive discussion between the presenters and the audience and reaching an agreement on the current and future challenges for the development of this field. The session also served as a networking event as technical discussions continued after the presentations concluded. It was also a useful networking opportunity, bringing together industrial and academic groups, hopefully paving the way for future technology transfer. We aim to continue this effort within HiPEAC, involving the same partners and presenters, but also trying to reach more people working on interconnects worldwide.

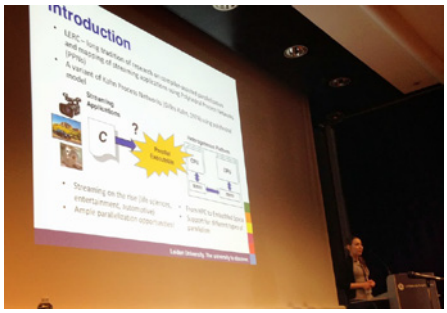
MAKING COMPUTER ENGINEERING A SCIENCE

The purpose of this thematic session was to bring together researchers interested in collaborative systematization and unification of the design and optimization of computer systems combined with a new publication model where experimental results are validated by the community. The reader is referred to the companion article in this newsletter, by Grigory Fursin, specially devoted to this thematic session.

EUINCOOP-HIPEAC SESSION: EURO-INDIA COLLABORATION IN ADVANCED COMPUTING SYSTEM RESEARCH IN THE HORIZON 2020

A special thematic session was devoted to the EUINCOOP supporting action within the EU FP7 framework, whose main objective is to strengthen collaboration between Europe and India in the field of Computing systems research, with the help of experts from both regions. The reader is referred to the companion article "Euro-India Collaboration in Advanced Computing System Research in Horizon 2020" in this newsletter, by Sathya Rao, specially devoted to this thematic session.

As a final note for this article, I just want to stress the importance of this HiPEAC-3 instrument to promote your research areas in the HiPEAC community, to share your own research results, and to build a network of researchers from which you can form a consortium for a future project proposal. Volunteering to organize a thematic session is an opportunity to contribute to the HiPEAC community, helping the HiPEAC network to work on



Thematic session on "Hybrid Programming Models and Optimizations for Heterogeneous Many-cores"

the challenges identified in the HiPEAC roadmap. I would like to congratulate the organizers of the Dynamic Compilation session for the excellent idea of conducting a survey across all talks in their session. All speakers were asked ahead-of-time to answer the same set of questions, to classify/differentiate their dynamic optimization approach. The answers were collected, forming a comparative summary, and presented at the end of the session. Being innovative in the organization of these sessions, escaping from the "traditional" format will be very welcomed. Thanks in advance for submitting a proposal in the forthcoming calls for thematic sessions.

Eduard Ayguadé, BSC / UPC, Spain

THEMATIC SESSION ON "MAKING COMPUTER ENGINEERING A SCIENCE": CLEANING UP THE MESS!

The purpose of this second thematic session held during the spring HiPEAC computing week in Paris was to bring together researchers interested in collaborative systematization and unification of the design and optimization of computer systems, combined with a new publication model where experimental results are validated by the community.

During the first part of the session, we had four exciting talks. Prof. Bruce Childers and Prof. Alex Jones from the University of Pittsburgh presented the long term OCCAM initiative recently started in the USA for Open Curation for Computer Architecture Modeling, with an ambitious goal to build a common collaborative infrastructure and repository for reproducible research and development in computer architecture modeling. Prof. Vittorio Zaccaria from the Politecnico di Milano presented ideas on combining social networking and public rankings to speed up and improve peer reviewed publishing. Dr. Christian Bertin and Dr. Christophe Guillon from STMicroelectronics presented the CARE tool (Comprehensive Archiving for Reproducible Execution) to create a compact archive of files necessary to reproduce experiments. Prof. Christophe Reichenbach presented the STEP project (Software Tools Evaluation Platform) to enable continuous and systematic tools reviews by the community.

In the second part, I presented my long-term vision and the third version of the public cTuning.org repository and plugin-based infrastructure (Collective Mind) to address some of the above challenges through crowd-sourcing, online auto-tuning and machine learning. In this cooperative approach, complex systems are gradually decomposed into simpler universal learning components (plugins) connected to Web and exposing tuning choices, properties and characteristics at multiple granularity levels to enable continuous tuning, learning and prediction of program and system behavior while utilizing any available mobile, cluster or cloud computer services. Such a collaborative approach allows the community to continuously validate, systematize and improve collective knowledge about computer systems, and extrapolate it to build faster, more power efficient and reliable computer systems. Furthermore, it should be able to suggest where researchers and engineers should focus their effort and creativity when designing or optimizing computer systems, thus boosting innovation and dramatically reducing development and optimization costs and time to market for new systems.

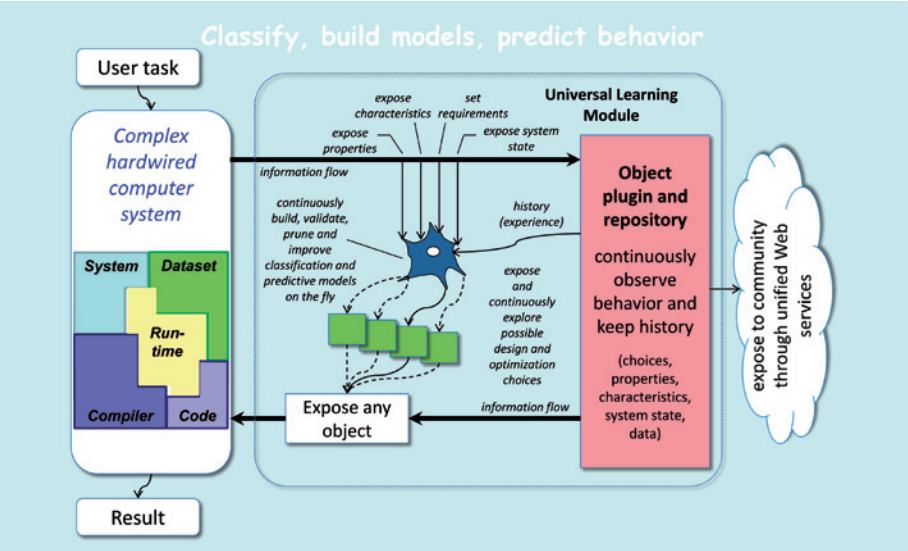
At the end of the session we identified the following next actions:

- Coordinate effort between HiPEAC and OCCAM
- Open Collective Mind repository with multiple benchmarks, codelets, data sets and models for the next event
- Prepare first pilot workshop where experimental results are validated by the community
- Reward not only reproducibility of new results, but also public implementation and validation of older techniques
- Address variation in experimental results across users during validation and ranking
- Allow to publish negative experimental results to avoid pitfalls in the future

I would also like to thank Markus Puschel, Olivier Zendra, Daniel Gracia Perez, Hans Vandierendonck, Gert Jervan, Ayal Zaks, Zbigniew Chamski, Koen De Bosschere, and many others for their suggestions and feedback.

Extra notes and all presentations are available on-line at http://www.hipeac.net/thematic-session/making-computer-engineering-science. If you have suggestions or interested to join this effort, please get in touch.

Grigori Fursin, INRIA, France



Collective Mind Infrastructure and Repository to crowdsource characterization and tuning of computer systems

EURO-INDIA COLLABORATION IN ADVANCED COMPUTING SYSTEM RESEARCH IN THE HORIZON 2020

EUINCOOP is a supporting project within the framework FP7 with an objective of developing closer collaboration across Euro-India research community addressing Computing systems research, in consultation and collaboration with experts in both regions. Since the start of the project in Oct. 2011, the project has compiled state of the art activities in both regions, identified key actors and policy directives as well as funded projects, so that reasonable collaboration can be proposed for joint activities between Europe and India. They presented these results in multiple events with experts participation from both regions (HIPEAC event, Gothenburg; HIPC 2012, Bangalore; ITBiz2012, India; HIPEAC events in Paris 2012 &2013). The results are compiled in their deliverables (D2.2 and D3.2) available in the project website www.EUINCOOP.eu as public deliverables. The latest roadmap document and proposed activities in the timeframe of Horizon 2020 were presented in the recent HIPEAC event in Paris on 2 May 2013 and the presentation is also available at HIPEAC website, which is frequently visited by the research community. The presentation included the profiles of both regions in terms of culture, knowledge resources and priorities identified by Indian Government and the European Commission for advancing computing systems research towards socio-economic development of their respective citizens.

Computing technology has entered a new phase due to fast paced evolutions in following key areas:

- Multicore and manycore processors including heterogeneous systems with various types of on-chip or off-chip accelerators.
- Software is becoming an important part of all kinds of computing systems
- Mobile devices like smartphones and tablets have emerged as the new "general-purpose" computing devices providing cloud access to millions of citizens and business.
- Knowledge mining is becoming a key enabler for industry and applications are becoming increasingly data-centric: Server farms, compute servers, HPC systems converging.
- Computing infrastructures rely on components more and more from the mobile world.
- System software for server farms is increasingly becoming more comlex
- Energy and cost efficiency are becoming as important as processing power.

Based on the analysis done across the full spectrum of activities, the SWOT (strength, weakness, opportunities and threats) analysis addressing the Euro-India collaborative issues in the development of next generation advanced computing systems research was presented.

A key challenge in advanced computing system research ahead of both communities is that of mastering parallelism, concurrency, and heterogeneity on all level from hardware, to system software, to services, and to applications.

The Roadmap document towards Euro-India collaboration in computing system research developed in the project shows that the number and complexity of the research challenges shared by Europe and India provides a clear indication that both regions could substantially benefit from a more collaborative approach to government funded computing systems research. With European strength in Hardware and Indian Strength being in software applied in developing more useful computing systems applications, the opportunity for a coordinated effort in computing systems research has perhaps never been greater as both Europe and India are each in the very early stages of implementing new multiyear programmes for funding technology research, are seeing new opportunities to benefit from the changing landscape of computing technologies, and each have referenced the importance of international collaboration as part of their multiyear funding strategies. These new circumstances bode well for being able to establish a genuine joint effort between Europe and India in addressing computing systems research technologies that are strategic to each region.

The EU-INCOOP partners have identified seven areas of shared interests in computing systems research that would substantially benefit Europe and India and are aligned with the strategies of the government funding programmes established in each region.
The most substantial computing systems research and technology challenges that have been identified as being common to both Europe and India are the following:

- Software for emerging platforms
- Software for internet based systems
- Software for Big Data
- System software for enterprise
- Network embedded system interoperability
- Software for social computing
- HPC Technology Platform

Within each area the EU-INCOOP project has indicated several specific technology topics for collaborative research. The technological and scientific challenges identified are substantial and the resources required to address all of the shared challenges would likely far exceed the combined funding resources that could possibly be allocated for joint initiatives by the two regions. In this context EUINCOOP project partners are still working towards narrowing down the key areas of research within the framework of the seven identified challenges for recommending the joint Euro-India research projects in the framework of Horizon 2020.

For more information contact: sathya.rao@kyos.ch or visit project website: www.euincoop.eu

Sathya Rao, KYOS Technologies, Switzerland

A SELF-AWARE PROSPECTIVE ON THE DESIGN OF NOVEL COMPUTING SYSTEMS

The HiPEAC Mini-Sabbaticals Program supported Marco Santambrogio's visit at MIT

The resources available on a chip, the level of integration and the speed of components have increased dramatically over the years. Semiconductor technology offers billions of transistors on a chip, the level of integration and the speed of components have increased dramatically over the years, and advancements show no sign of abating. Post-silicon technologies such as graphene electronics could offer even more industrially viable computing power within years. Heterogeneous, adaptable multicore systems can be considered the established trend in modern computing architectures. Runtime reconfigurable elements can be combined together with heterogeneous processing elements and many cores on a chip by processor designers. In recent times, unfortunately, these advancements have not resulted in a proportional increase in performance or other measures of interest to users, furthermore such systems also pose new research questions to be answered, i.e. will current processor interconnection mechanisms scale to thousands of cores? How can the runtime behaviour, which cannot be fully understood at design time, be captured to be reflected into a physical implementation to extract high performance from the underlying hardware architecture?
Furthermore, it is no longer practical for an average programmer to balance all of the system constraints and produce applications that perform well on a variety of machines, in a variety of situations. Within this context, this is the right time for a fresh approach to the way systems are designed and used. Self-Aware computing is a research area aimed at leveraging the new balance of resources to improve performance, utilization, reliability and programmability, overcoming the burden imposed by the increasing complexity and the associated workload of modern computing systems.

HiPEAC supports the mini-sabbatical of Dr. Santambrogio at MIT to investigate how self-awareness combined with adaptability will enable novel computing systems to change features of their behaviour towards a goal in a way completely different from what happens nowadays with systems upgrading, where the new behaviour is uploaded from outside, depending on human design effort and intervention. Behaviour adaptation will rather be intrinsically embedded in the device, and continuously working according to the target objective and to the inputs coming from the external environment. In the most general case, goals can be descriptions of functionalities to offer, non-functional constraints or objectives to maximize, or a mixture of both. At every moment, the system will be able to compute how close it is to its goals.

Marco Santambrogio (top row, fourth from the left) with the participants of the workshop at MIT

This will be possible since self-aware computer systems will be able to configure, heal, optimize, improve interaction and protect themselves, exploiting abilities that allow them to automatically find the best way to accomplish a given goal with the resources at hand. Within this context, imagine a revolutionary computing system that can observe its own execution and optimize its behaviour around the external environment, user's and application's needs. Imagine a programming capability by which users can specify their desired goals rather than how to perform a task, along with constraints in terms of energy budget, time constraints. Imagine further a computing chip that performs better, according to a user's preferred goal, the longer it runs an application. At the moment, we cannot even imagine all the potential benefits of self-aware devices in real-life applications, e.g., for applications of pervasive computing/control among which, for instance, medical pilot plants, neurological control systems, adaptive communication infrastructures.

At the end of the mini sabbatical, Dr. Santambrogio with Prof. Srini Devadas organized a 2-day workshop at MIT to present the research work done by the two institutions, Politecnico di Milano and MIT, and they used this event as a way to strengthen/reinforce the collaboration between their research groups. Researchers from both institutions had the chance to present their works and a final brainstorming session posed the bases for future collaboration in the design of novel computing systems exploiting self-aware capabilities.

Marco Santambrogio, Politecnico di Milano, Italy

ACM EUROPE: A EUROPEAN PERSPECTIVE WITHIN ACM

Association for Computing Machinery

ACM Europe aims to strengthen the European computing community at large, through its members, chapters, sponsored conferences and symposia.
Together with other scientific societies, it helps make the public and decision makers aware of technical, educational, and social issues related to computing.
The ACM Europe Council brings a unique European perspective inside ACM and helps increase visibility of ACM across Europe, through:

- Participation of Europeans throughout ACM
- Representation of European work in ACM
- Awards and Advanced Membership Grades
- Holding high-quality ACM conferences in Europe
- Expanding ACM chapters
- Strong co-operation with other European
- scientific societies in computing

ACM - WORLD'S LARGEST EDUCATIONAL AND SCIENTIFIC COMPUTING SOCIETY

ACM strengthens the computing profession's collective voice through strong leadership, promotion of the highest standards, and recognition of technical excellence. ACM supports the professional growth of its members by providing opportunities for life-long learning, career development, and professional networking.
ACM is present in Europe with more than 16,000 members and more than 70 chapters. 24 ACM Turing Awards and other major ACM awards have gone to individuals in Europe. 392 Europeans have received an Advanced Membership Grade.

ACM-W EUROPE

ACM-W Europe aims to advance the status of women in computing by raising awareness of career options; providing a platform for sharing resources, ideas and experiences; establishing partnerships with similar existing organizations in Europe; and working with the EU and European Commission on programs for women in computing.

ACM EUROPE TODAY

The ACM Europe Council serves a growing constituency by:

- Increasing the number of chapters, particularly for students
- Expanding interest in nominations for ACM professional awards and distinguished member grades
- Engaging ACM's Special Interest Groups to focus on Europe when planning conferences and major events

Contact us at: acmeurope@acm.org

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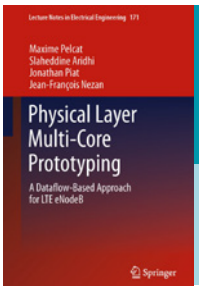
- Mateo Valero, U. Politecnica de Catalunya, Spain
- Alexander Wolf, Imperial College London, UK

A special reception at ECRC recognized European ACM Fellows. Back row, from left to right: Per Stenström, ACM Vice President Alexander Wolf, John T. Richards, Keith J. Van Rijsbergen, Ricardo Baeza-Yates, Mateo Valero, Ronald H. Perrott, Bertrand Meyer, Lars Arge, Christian S. Jensen
Front row, from left to right: Walter F. Tichy, Peter B. Key, Jürg Nievergelt, Carlo Ghezzi, Leonid Libkin, Maurizio Lenzerini, former ACM president Dame Wendy Hall, Vicki Hanson



BOOK ON PHYSICAL LAYER MULTI-CORE PROTOTYPING: A DATAFLOW-BASED APPROACH FOR LTE ENODEB

Maxime Pelcat, Slaheddine Aridhi, Jonathan Piat, Jean-Francois Nezan

Base stations developed according to the 3GPP Long Term Evolution (LTE) standard require unprecedented processing power. 3GPP LTE enables data rates beyond hundreds of Mbits/s by using advanced technologies, necessitating a highly complex LTE physical layer. The operating power of base stations is a significant cost for operators, and is currently minimized using state-of-the-art hardware solutions, such as heterogeneous distributed systems. The traditional system design method of porting algorithms to heterogeneous distributed systems based on test-and-refine methods is a manual, and therefore time consuming, task.

Physical Layer Multi-Core Prototyping: A Dataflow-Based Approach for LTE eNodeB provides a clear introduction to the 3GPP LTE physical layer and to dataflow-based prototyping and programming. The difficulties in the process of 3GPP LTE physical layer porting are outlined, with particular focus on automatic partitioning and scheduling, load balancing and computation latency reduction, specifically in systems based on heterogeneous multi-core Digital Signal Processors. Multi-core prototyping methods based on algorithm dataflow modeling and architecture system-level modeling are assessed with the goal of automating and optimizing algorithm porting.

With its analysis of physical layer processing and proposals of parallel programming methods, which include automatic partitioning and scheduling, Physical Layer Multi-Core Prototyping: A Dataflow-Based Approach for LTE eNodeB is a key resource for researchers and students. This study of LTE algorithms that require dynamic or static assignment and dynamic or static scheduling, allows readers to reassess and expand their knowledge of this vital component of LTE base station design.

HIPEAC BOOTH AT DATE 2013

Spreading HiPEAC through the scientific community

The DATE (Design, Automation and Test in Europe) conference attracts every year a large number of companies and academic institutions, and is therefore the optimal opportunity to promote HiPEAC to the scientific and industrial community. The 2013 DATE Exhibition took place from March 19-21 in Grenoble, France. As in past years, the Institute of Communication Technologies and Embedded Systems (ICE) of RWTH Aachen University organized a HiPEAC booth at DATE in order to present current activities within the project and to introduce HiPEAC to non-member conference participants.

Among the HiPEAC members, interest was focused on the new version of the roadmap towards Horizon 2020 and details about upcoming events, such as the Computing Systems Week in Paris. Non-members were primarily interested in understanding the "business model" behind the network and how their participation could potentially benefit their personal research. The frequent networking, academic and educational events sponsored by HiPEAC were of constant interest to DATE participants, as these meetings create an opportunity to get in touch with researchers involved in similar or complementary fields of research. Forthcoming events such as the Fall Computing System Week 2013 in Tallinn were announced to all visitors, as well as the upcoming ACACES Summer School in Fiuggi and the 2014 HiPEAC Conference in Vienna.

Although the main focus of the booth was to present the project and its activities, it has been our tradition to showcase research being developed by the HiPEAC partners. Results from the field of Electronic System Level (ESL) Power Estimation were presented by RWTH´s Stefan Schürmans, who has been working together with an industrial partner on the development of new techniques to speed up power estimation at high levels of abstraction. The inclusion of academic content on the booth proved to be another major attraction, and was the focus of several discussions. As a consequence, a joint meeting was held after the conference between ICE and the Oldenburg Research and Development Institute for Information Technology Tools and Systems (OFFIS), in which collaboration projects in the power estimation field were discussed. This again shows the benefit of promoting HiPEAC in all the main conferences as a valid way to further stimulate networking among the scientific community.

Juan Eusse, Stefan Schürmans and Maria Rodriguez at DATE 2013

Maria Rodriguez and Juan Eusse, RWTH Aachen University, Germany

EUROPEAN LLVM CONFERENCE 2013

How collaborative work on an open source project enables innovation

At the end of April (28-29) the European LLVM Conference 2013 took place in Paris right before the HiPEAC Computing Systems Week. Continuing the steep growth of the previous years, the third incarnation of Euro LLVM hosted two parallel tracks, two keynotes, ten talks, two tutorials, seven lightning talks and ten posters. In the historic buildings of École Normal Supérieure, over 170 attendees from industry and research painted a lively picture of the LLVM community. The conference content has been made available online.

Having started as a masters thesis back in 2001, LLVM is nowadays a vibrant open source project collaboratively developed by research, industry and independent contributors. It provides with clang a leading C/C++ compiler, and the project's focus on the development of modular and reusable compiler components has led to a far wider impact. Numerous industry products have been developed on top of LLVM and its broad use in research has led to over 1000 publications citing LLVM.

The Euro LLVM conference featured hot topics and recent innovations in and around LLVM. The two keynotes discussed ideas that currently influence design choices in the very core of LLVM. Chandler Carruth's presentation Optimization in LLVM illustrated open optimization challenges at the compiler IR level. Jakob Olesen explained modern CPUs and how they influence the design of LLVM's backends. The subsequent presentations then gave insights into the different areas of the LLVM ecosystem. Starting with a tutorial about the C/C++ AST used by clang, several talks discussed how to perform source-to-source transformations, how to automatically format source code, and how to easily extend C/C++ with pragmas. Closely related was the talk about OpenMP in clang, which included the announcement of the first open source release of the Intel OpenMP run-time library. A diverse set of talks about debug information, linking, tracking of uninitialized values, decompilation and the LLVM assembler followed. The talk about the status of the LLVM POWER processor gave a developer's perspective on the differences between developing for gcc and LLVM. Posters and lightning talks supplemented the talks and gave an impression of the diverse set of projects developed in the LLVM community.

Besides the technical presentations, a core goal of the conference was to strengthen the European LLVM community and its connections to overseas contributors. We have seen many lively discussions taking place during the coffee breaks, the poster session as well as the dinner cruise in front of the historic Paris. Those discussions will hopefully not only simplify the day to day work on the shared source code, but also lead to new collaborations and technology transfers between the industrial and academic users of LLVM - in the best case again resulting in innovative contributions to the open source base of the LLVM Project.

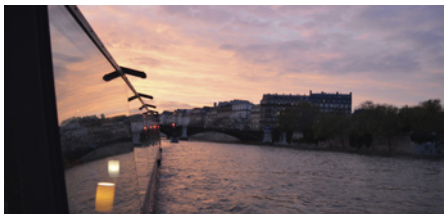
Overall, the conference was a large success. In an anonymous survey taken at the end of the conference, 98% of the respondents rated the overall conference experience good or excellent with positive feedback for the venue and the networking opportunities. Excellent feedback was given not only for the dinner cruise, but more importantly all content received more than 90% positive votes with an overwhelming 100% good or excellent votes for the talks themselves. Such a success was only possible with the help of our sponsors and the LLVM community. We would like to thank all of them and are looking forward to Euro LLVM 2014.

For more info, visit
http://llvm.org/devmtg/2013-04/

Tobias Grosser, INRIA, France

École Normal Supérieure

Eric Christopher's presentation



Evening social on the river Seine

MATEO VALERO AND TONY HOARE, AWARDED HONORARY DOCTORATES BY THE UNIVERSIDAD COMPLUTENSE DE MADRID

Director of the Barcelona Supercomputing Center-Centro Nacional de Supercomputación (BSC-CNS) Mateo Valero and Microsoft senior researcher Sir Charles Anthony Richard Hoare are the first computer scientists to have been awarded an honorary doctorate by the Universidad Complutense de Madrid (UCM). With this award, proposed by the School of Computer Sciences and coinciding with the Alan Turing Year, the UCM recognizes their unique contributions to computer science. The two new doctors used their acceptance speeches to highlight not only the spectacular advances in computing in recent decades, but also the role that computing will play in the future.

Hoare stressed the importance of offering a computer science education founded on a solid basis that takes into account not only the latest developments, but also unifying theories. In this manner, Hoare's speech is consistent with the work he's committed himself to in recent years that have culminated in the programming laws he has recently announced.

Computer Science Professor Ricardo Peña Marí, Hoare's sponsor, praised the British computer scientist, stating that "his contributions have been instrumental in making computer programming a scientific discipline; starting from an initial situation in which programming was more like an art, a craft, rather than a science." Peña was referencing Quicksort, Hoare's sorting algorithm, the Hoare logic for verifying program correctness and the formal language Communicating Sequential Processes (CSP) to specify the interactions of concurrent processes, some of Hoare's most well-known work.

Francisco Tirado Fernandez, Professor of Architecture and Computer Science at UCM presented the laudation praising Valero's contributions to the field of computer architecture, particularly in the areas of vector, out-of-order and VLIW processors. Tirado highlighted the BSC-CNS Director's valuable contributions of seminal ideas to the field of High Performance Computing (HPC) and their impact on academia and industry. He also highlighted Valero's technology transfer activities including establishing joint research centers and collaboration agreements between the BSC-CNS and companies such as IBM, HP, NVIDIA, Intel and Microsoft.

Dr. Valero stressed the need for science to lead the economic recovery process. "Good training and research are the most direct way to get out of the crisis as soon as possible", said Valero, who encouraged researchers to develop ideas that can contribute to building wealth in our societies.

THEMATIC QUARTER ON COMPILATION, LYON APRIL-JULY 2013

The MILYON labex is a funding agency whose goal is to federate the mathematics and fundamental computer science in Lyon and to strengthen international relationships, through the organization of thematic quarters, gathering world experts on specific subjects. In this context, the Compsys team organized, from April to July 2013, a thematic quarter on compilation techniques (http://labexcompilation.ens-lyon.fr), with a special focus on the interactions with languages and architectures for high performance computing, consisting of four scientific events.

- The French compilation days (http://labexcompilation.ens-lyon.fr/compilation-days), April 4-7, 2013 in Annecy, the bi-annual meeting of the French community in compilation.
- A spring school on polyhedral code analysis and optimizations (http://labexcompilation.ens-lyon.fr/polyhedral-school), May 13-17, 2013, in St Germain au Mont d'Or, the first international school on the polyhedral model and related optimizations. This school attracted 55 participants, mainly from Europe and the US, and it covered polyhedral scheduling theory, algorithms and modeling with integer sets and relations, abstract interpretation, polyhedral compilation for distributed

platforms, array region analysis, vectorization and SIMD optimizations, through courses given by S. Rajopadhye (Colorado State Univ.), P. Feautrier (ENS-Lyon), L.-N. Pouchet (UCLA), S. Verdoolaege (ENS Paris), A. Miné (ENS Paris), U. Bondhugula (IIS Bangalore), A. Darte (CNRS Lyon), B. Creusillet (Silkan), P. Sadayappan (Ohio State Univ.), N. Vasilache (Reservoir Labs).

- A dive in languages for high-performance computing (http://labexcompilation.ens-lyon.fr/hpc-languages), June 29-July 2, 2013 in Lyon, organized as a set of long keynotes on CAF (Coarray Fortran), UPC (Unified Parallel C), X10, Chapel, OpenACC & OpenHMPP, Liquid Metal, OmpSs, OpenStream, and some DSL approaches. The keynotes are given by a panel of international experts on compilation for high-performance computing such as J. Mellor-Crummey and V. Sarkar (Rice), K. Yelick (Berkeley), R. Schreiber (HP Labs), B. Chamberlain (Cray), D. Grove and R. Rabbah (IBM), A. Cohen (Inria), and R. Badia (UPC Barcelona).
- CPC'13, the 17th international workshop on compilers for parallel computing (http://labexcompilation.ens-lyon.fr/cpc2013), July 3-5, 2013, in Lyon, a venue that is held every 18 months in Europe since 1989 and that encompasses all hot areas of parallelism and optimization linked to compilers. The program consists in 30 talks, from the international community on compilers for HPC (from Japan & Taiwan to the USA, and of course Europe).

Sponsors & support: Labex MILYON, University of Lyon 1, ENS-Lyon, Inria, CNRS.

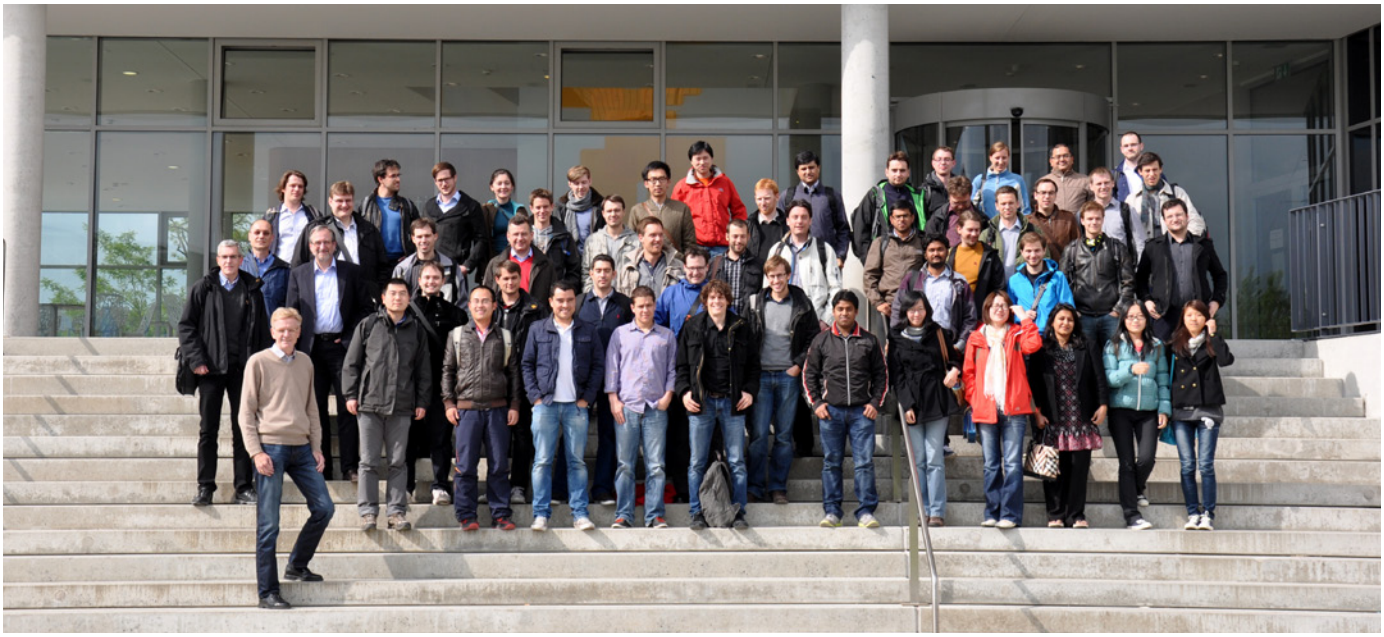
Alain Darte, CNRS, Compsys team, France

JOINT SEMINAR: TECHNICAL UNIVERSITY MUNICH & RWTH AACHEN UNIVERSITY

On the 26 May 2013, members of the Institute for Communication Technologies and Embedded Systems (ICE) of RWTH Aachen University have been invited for a whole-day joint technical seminar together with the Technical University of Munich (TUM). This seminar was another in a chain of events co-organized by RWTH Aachen during the past years, made possible by the mobility initiative of HiPEAC. As reported in several previous articles of the HiPEACinfo newsletter, prior technical get-togethers enabled ICE to meet and discuss with top research members of Edinburgh University, Imperial College London, Tampere University of Technology and Poznan University of Technology. The 2013 event was hosted by Prof. Herkersdorf, Prof. Stechele and Dr. Wild of the Chair for Integrated Systems and Prof. Chakraborty of the Chair for Real-Time Computer Systems of the TUM.

The agenda started with introductory presentations held by Prof. Herkersdorf and Prof. Chakraborty, followed by technical talks of several members of the two hosting chairs regarding topics of HW/SW System-Engineering, MPSoCs, NoCs, novel architectures, methods and tools, also with special focus on the automotive domain promoted by the major local automotive research and manufacture companies. After a short lunch break, the seminar continued with an introduction to ICE held by Prof. Ascheid and Prof. Leupers. This was followed by several technical talks covering the topics of ESL Power Estimation, MPSoC Debugging, High-level Fault Injection, ASIP-ASIC Efficiency Gap and Multi-Mode MIMO Detection. The agenda finished with a joint discussion about possible future cooperation, conjoined research possibilities, further workshops and seminars, and a possible HiPEAC contribution.

Róbert Lajos Bücs, RWTH Aachen University, Germany



Joint picture with the members of both TU Munich and RWTH Aachen

FP7 EUROCLOUD PROJECT

Energy-conscious 3D Server-on-Chip for Green Cloud Services

Project Name: EuroCloud

Project coordinator: Emre Ozer, ARM Research

Duration: 36 months

Partners: ARM (UK), Nokia (FI), Cancer Research (UK), IMEC (BE), EPFL (CH), University of Cyprus (CY).

Start date: June 2010

URL: www.eurocloudserver.com

eurocloud

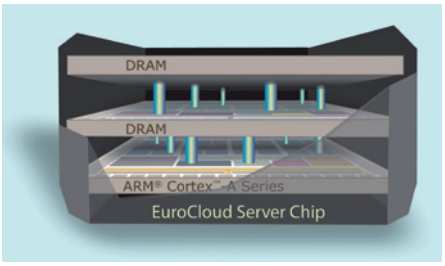
Every year, data centres produce carbon dioxide emission levels approaching that of the entire Netherlands. The majority of data centres are powered by carbon-based fuels, and only a fraction of them are powered by a mixed of carbon and renewable energy sources or 100% renewable energy. Data centres are unlikely to switch to 100% renewable energy because of high costs, unless their owners make significant investments in renewable energy. Thus, it is instrumental that the high energy consumption and cost of data centres must be addressed at the design level. Servers are responsible for the largest energy consumption and capital cost in data centres. A server is a computer with four main components - server chip, DRAM, networking gear and storage. The server chip is the key contributor to server energy consumption as well as the entire data centre, ranging from 20-30%. In addition, the cost of these server chips can be extremely high, resulting in extra costs for the data centre owners.

EuroCloud is an FP7 Computing Systems STREP project that started in January 2010. The project is led by ARM, with the rest of the consortium consisting of Cancer Research UK, Nokia, IMEC, EPFL and University of Cyprus. The EuroCloud project aims at using more energy-efficient microprocessor chips in servers and datacentres. We have been investigating "server chips" based on the ARM microprocessor architecture – the same architecture used in 95% of all mobile phones, tablet computers and other battery-operated portable devices. EuroCloud is demonstrating the use of ARM-designed energy-efficient chips in servers and datacentres. The project is testing commercial web hosting demonstration and Cancer research software to validate the improvement in TCO (Total Cost of Ownership).

In the EuroCloud project, we take a new approach in the future of ARM-based servers. We are developing a new ARM-based energy-efficient chip virtual prototype specifically designed for servers. We call it "3D Server-on-Chip" built integrating many ARM processors with a memory to provide a very dense power-efficient server. EuroCloud targets a 10x improvement in energy-efficiency compared to current state-of-the-art servers. Thus, EuroCloud will enable the data centre owners to build very efficient, environmentally clean and compact data centres in Europe.

PROJECT ACHIEVEMENTS

The project has researched a number of directions simultaneously in order to be able to subsequently develop much more power-efficient servers. Research is in the following areas:



- We have developed a virtual prototype of the 3D server-on-chip consisting of many-core ARM-based logic die 3D-integrated with WideIO DRAM die, and modelled the 3D chip using the virtual-physical prototyping tools driven by the cloud workloads
- We have developed a Scale-out processor architecture in which the chip is divided into independent clusters or pods, and each pod has multiple ARM cores integrated with their own caches and memory interfaces
- The project has built TCO (Total Cost of Ownership) models spanning the chips to the datacentres. They help us understand how design decisions at the chip level impact the datacentres in terms of economics, power, and CO_2 emissions
- The project has built a workload suite called "CloudSuite" representing may real cloud and scale-out applications used in today's data centres
- We have investigated new ways of building future reliable chips
- We have validated the TCO, power/performance with commercial web hosting and Cancer research applications using first commercially ARM-based server systems

Emre Ozer, EuroCloud Project Coordinator

ARM	ARM – Processor Company (UK)	Low-power Server-on-Chip Architectures
CANCER RESEARCH UK	Cancer Research UK – Research Institute (UK)	Evaluation of Commercial Low-power ARM processor based servers in Green Data Centers
NOKIA Connecting People	Nokia – Mobile Phone Company (Finland)	
imec	IMEC – Chip Manufacturing Research Institute (Belgium)	3D Chip Virtual Prototypes
EPFL	EPFL – University (Switzerland)	On-chip Memory Hierarchy and Cloud Workload Dev.
University of Cyprus	UCY – University (Cyprus)	Server Chip Reliability, Fault Tolerance & TCO Models

PROJECT DISSEMINATION

- The EuroCloud project was invited to the "Made in Europe" event in the European Parliament in Oct-2012. Only nine EC-funded ICT projects are invited out of more than 1000 currently running projects.
- In September 2012, the European Commission made a press release on EuroCloud "Digital Agenda: EU-funded research to make the cloud greener"
- EuroCloud has been in the media since 2010, for example:
  - Energy-conscious 3D Server-on-Chip for Green Cloud Services (FP7 Project No:247779 – "EuroCloud") Press Release, ARM Press Release
  - "ARM to lead EC funded EuroCloud green data centre research initiative", eetimes
  - European Commission (EC) declares EuroCloud as one of the flagship projects in Europe, Hipeac Press Releases, 2012
  - "Scale-out Processors", ACM TechNews
  - "Every cloud has a green lining", Cordis Technology Marketplace
- We have published over 25 papers during the course of the project many of which are published in top conferences/ journals, e.g. ISCA, Micro, ASPLOS, IEEE Micro, DATE, ICCD and ISPASS.

FP7 2PARMA PROJECT: A SUCCESS STORY

Parallel paradigms and run-time management techniques for many-core architectures

Project Name: 2PARMA

Project Coordinator: Prof. Cristina Silvano, Politecnico di Milano

Duration: 39 months

Partners: Politecnico di Milano (IT); STMicroelectronics (IT/FR); Fraunhofer - HHI (DE); IMEC (BE); ICCS (GR); RWTH Aachen (DE); Synopsys (BE).

Start Date: January 2010

Url: http://www.2parma.eu

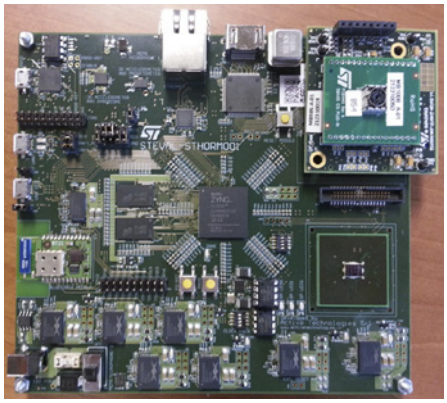
2 PARMA

KEY INNOVATION

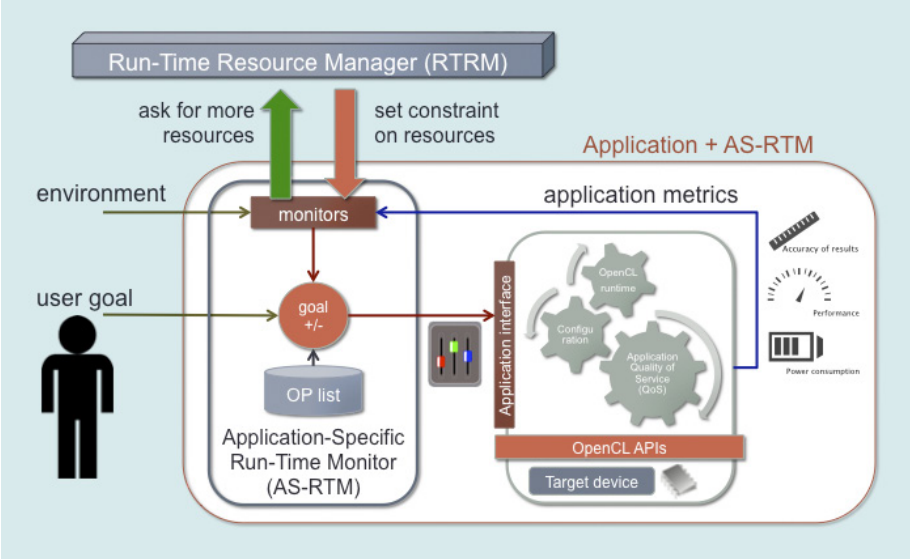
The current trend in embedded computing architectures to increase the number of processing cores (scaling to 64+ cores in the near future) requires a global rethinking of software and hardware design methodologies, due to the increased complexity of design and runtime management of applications that fully exploit the computational parallelism. The 2PARMA project (www.2parma.eu) provides tools and software components for application development and execution on such many-core systems. The proposed approach enables efficient run-time resource management (with a power saving greater than 8% and, in some cases, a 5x improvement of the energy per task execution compared with the baseline strategy), while ensuring the desired Quality of Service (QoS) in multi-application scenarios.

TECHNICAL APPROACH

The project tackles the issue of programmability of Many-Core Computing Fabrics (MCCFs) at both the programming language and the Operating System level. The project defined a compilation tool-chain to support parallel programming, based on both the component-based and the single-instruction multiple-thread (OpenCL) approaches. The project also provides a run-time resource management framework driven by design space exploration to automatically generate power-delay operating points for multiple applications running on MCCFs. The project developed policies to manage the system resources taking into account the QoS requirements imposed by the application, while optimising the resource usage for system-wide performance and energy consumption goals. Continuous adaptation and run-time management require profiling information to take effective and timely decisions. 2PARMA goes beyond traditional design space exploration by defining a methodology to provide synthetic information about the points of operation of each application with respect



P2012/STHORM evaluation board



Application adaptivity through AS-RTM and RTRM

to the subsets of resources available to it. Moreover, application-specific monitoring techniques have been developed, and the issues of stability and robustness of control have been addressed. All concepts and components developed in the project have been evaluated by demonstration on innovative hardware platforms provided by the partners, including Platform 2012/STHORM, an early MCCF prototype provided by STMicroelectronics. To ensure a wide range of application scenarios comprising the typical computation-intensive workload of a computing system, the following applications have been used and customized by means of the developed techniques: Scalable Video Coding, Cognitive Radio, and Multi-View stereo matching.

SCIENTIFIC, ECONOMIC AND SOCIETAL IMPACT

The project improved the perception of the trade-offs involved in switching periodically to better technologies, thus achieving faster time-to-market and providing more user-friendly tool-chains to customers, through the development of an LLVM-based compiler technology for P2012/STHORM. Several project outcomes, such as the BBQ Run-Time Resource Manager, the Dynamic Memory Manager and the Multi-View application, are mature enough to be used in an industrial context. STMicroelectronics directly benefits from the project through the ability to include project results in its P2012 SDK, but the public availability of research results and tools will benefit a wider industry and academic community.

COLLABORATION GRANT REPORT - SABELA RAMOS

Modelling Communication in Cache-Coherent SMP Systems with Xeon Phi

A HiPEAC Collaboration Grant enabled the three-month research visit of Sabela Ramos, a PhD student at the Computer Architecture Group (University of A Coruña, Spain). She visited Prof. Torsten Hoefler at the Scalable Parallel Computing Laboratory (ETH Zürich, Switzerland), from September to December 2012.

The project developed under this collaboration was focused on the analysis of shared memory communications in cache coherent systems, paying especial attention to the Xeon Phi [1] features in comparison with other multi-core architectures such as Intel Nehalem and Sandy Bridge, and the study of collective communication algorithms in this new system. This work was motivated by two main reasons. On the one hand, the generalization of multi- and many-core processors makes it necessary to provide tools and models to develop efficient and scalable communication algorithms for shared memory architectures. Moreover, most of these architectures are based on cache coherency protocols as the only means of communication between cores. On the other hand, early results and experiences with the new Intel Xeon Phi architecture, obtained during the first days of the research visit, were promising in terms of exploiting shared memory with MPI programming in manycore environments. The methodology used was the design of a set of benchmarks, extending existing ones [2] and implementing others, to characterize the communication costs and simplifying the resulting model as much as possible.

The result of this research work was the development of a communication model for cache coherent systems adapted to the Xeon Phi characteristics. This model enabled and guided the design of several efficient and optimized communication algorithms (broadcast, reduction and synchronization barrier) that outperformed the ones from Intel MPI and Intel OpenMP on Xeon Phi.

Due to the high interest in the Xeon Phi manycore accelerator and the high potential of the work undertaken during this visit, the outcome has already been accepted for publication at the HPDC 2013 Conference: "Modeling Communication in Cache-Coherent SMPSystems - A Case-Study with Xeon Phi".

Sabela Ramos, Universidade da Coruña, Spain

COLLABORATION GRANT REPORT - RAQUEL CONCHEIRO FIGUEROA

Real-time rendering of non-complex Bézier surfaces on the GPUs of handheld devices

Last summer, I had the opportunity to visit the UPC. While my PhD research is focused on the real time rendering of parametric surfaces on the GPU, under the supervision of Margarita Amor and Montserrat Bóo, thanks to the HiPEAC collaboration grant, I had the chance to work together with Marisa Gil and Xavier Martorell on the rendering capabilities of handheld devices. The market for handheld devices is nowadays one of the fastest growing technology markets. Graphics processing has become a significant factor on these devices, as consumers' expectations have increased, demanding high quality visual contents and complex render capabilities. Consequently, a new GPU generation has been specifically designed to fit in the

constraints of handheld devices: size and power-consumption. Hence, GPUs of these devices implement only a subset of the features available in commodity desktop GPUs.

GPUs are usually designed to work with triangles and vertices. However, these geometric primitives are not always the best option from a modeling point of view. Thus, the use of parametric surfaces to design complex and detailed models has widely spread in fields such as CAD/CAM, virtual reality, animation and visualization. Specifically, the Bézier representation has been widely employed in the designing of high quality complex models.

As the current GPUs of handheld devices implement a small set of features of desktop GPUs, none of the previous proposals can be computed on the GPU of a handheld device, as far as we know. However, our proposal tessellates parametric surfaces into high-quality triangle meshes that accurately represent complex surfaces and do not contain artifacts such as T-junctions or cracks. It is based on the utilization of parametric maps of virtual vertices, which makes it possible to work on GPUs with no primitive generator. Specifically, our design allows the efficient exploitation of the information stored in the GPU and the minimization of the CPU-GPU communications. Three main parameters are exposed to allow a fine tuning to the hardware resources available: maximum resolution level, number of surfaces to be rendered per draw call and number of draw calls per frame. In order to test our approach, we have designed an OpenGL ES implementation for Android systems and a full set of experiments to analyze features of current handheld GPUs. The tests were focused on locating the main performance bottlenecks and identifying possible enhancements and tuning opportunities.

As a result of our analysis, we have achieved real-time rendering of non-complex Bézier surfaces on the GPUs of handheld devices. Furthermore, we analyze the main features that could introduce architecture improvements in order to obtain real-time rendering or of complex parametric surfaces.

This work has been published as a full paper in the 21st International Conference on Computer Graphics, Visualization and Computer Vision 2013 (WSCG 2013).

Finally, I want to take this opportunity to thank HiPEAC as well as the UPC.

Raquel Concheiro Figueroa, Universidade da Coruña, Spain

INTERNSHIP REPORT - DANIEL HOFMAN

Video processing on many-core architectures based on Network on Chip

After the last summer I went for one semester to do part of my doctoral research at at the Universitat Politècnica de València (UPV), Spain. I am a student at University of Zagreb, Faculty of Electrical Engineering and Computing. For the last four years I have been working with my mentor prof. Mario Kovač. He founded the Multimedia and Computer Architectures Research Center at our faculty, where we are working on the newest approaches in the field of multimedia processing and processors which of course includes parallel processing and making everything go better and faster.

My focus in the lab is on parallel processing of multimedia on many-core processor architectures. Although the introduction of many-core architectures has provided more computing power it has also introduced problems of distribution of algorithms to multiple cores and problems of efficient routing of data between those cores, related to the Network on Chip. Future processors are likely to have hundreds of cores on a single chip which will, therefore, require complex and scalable routing algorithms for efficient data processing.

Prof. José Flich Cardo was my host at UPV, and he now is co-mentoring me in my research. During my stay in Valencia I was at *Departamento de Informática de Sistemas y Computadores, Grupo de Arquitecturas Paralelas (GAP)* working in a lively atmosphere, together with young and devoted researchers. They have developed a cycle-accurate flit-level Network on Chip simulator called *gNoCsim*. Using *Graphite* developed at *MIT* and *gNoCsim* I was analysing the on-chip network traffic generated by the video coding algorithms. It included simulations on processors with up to 64 cores using different routing algorithms such as *Dimension Ordered Routing, Logic Based Distributed Routing* and *Segment-Based routing*. Video coding was performed on sample animations coded with a parallelised version of H.264 encoder. Results of the simulations will be used in the continuation of the research for making optimised algorithms for network data routing in many-core Network on Chips.

After returning home, I switched from the Graphite to the Sniper simulator together with *gNoCsim* for simulating the network traffic on the desired network architecture. In April ITU-T finally approved the novel *High Efficiency Video Coding (HEVC)* as a standard, so I will also include it in my investigation.

sDoing research at *GAP* was a valuable experience that has widen my views on research and academic life. In addition to making a significant progress in my research I also got a different perspective on the organization of the University. I learned a lot about the Spanish language, and the culture and temperament of Spanish people.

Working in a foreign country for at least three months is an experience that will make anyone see his own country with different eyes and think about everything in a different way - from a slightly different perspective. For me it was also a great tutor that made me more focused on the things that I want and like.

Daniel Hofman, University of Zagreb, Croatia

A STRATEGY TO REDUCE INTERCONNECTION NETWORK POWER CONSUMPTION

Marina Alonso Diaz
Universidad Politécnica de Valencia, Spain
Advisors: Prof. Vicente Santonja and Prof. Pedro Lopez
June 2012

In this thesis, we propose a strategy to reduce the interconnection network power consumption. The proposed mechanism combines two alternative techniques: (i) dynamically switching on and off network links as a function of traffic, and (ii) dynamically setting the available link bandwidth as a function of traffic. In both cases, the topology of the network is not modified. Therefore, the same routing algorithm can be used regardless of the power saving actions taken, thus simplifying router design. Our results show that the network power consumption can be greatly reduced, at the expense of some increase in latency. However, the achieved power reduction is always higher than the latency penalty.

DESIGN OF EFFICIENT PACKET MARKING-BASED CONGESTION MANAGEMENT TECHNIQUES FOR CLUSTER INTERCONNECTS

Joan-Lluis Ferrer Perez
Universidad Politécnica de Valencia, Spain
Advisors: Assoc. Prof. Elvira Baydal, Prof. Antonio Robles and Prof. Pedro Lopez
December 2012

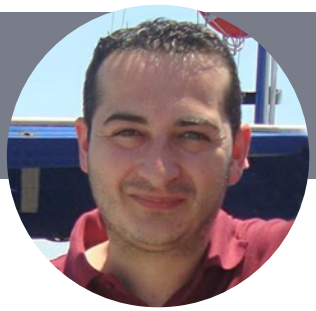
The aim of this dissertation is to analyze the different strategies to detect and correct congestion in multistage interconnection networks and propose new congestion management mechanisms targeted to this kind of lossless networks. The new approaches will be based on a more refined packet marking strategy combined with a fair set of corrective actions in order to make the mechanisms capable of effectively managing congestion regardless of the congestion degree and traffic conditions.

CODE GENERATION FOR GPU ACCELERATORS FROM A DOMAIN-SPECIFIC LANGUAGE FOR MEDICAL IMAGING

Richard Membarth,
University of Erlangen-Nuremberg, Germany
Advisor: Prof. Dr.-Ing. Jürgen Teich
May 2013

This thesis presents the HIPAcc framework for the automatic code generation of medical imaging algorithms on GPU accelerators. A domain-specific language (DSL) decouples the algorithm from its schedule. Together with domain knowledge and an architecture model, this enables an efficient mapping of the algorithm to a deep memory hierarchy as found in today's GPUs. Tailored code variants are generated for different target architectures, significantly improving the programmer's productivity. Compared to hand written codes, the performance of the generated low-level CUDA and OpenCL implementations is competitive with GPU accelerators from NVIDIA and AMD while preserving high portability.

EFFICIENT, SCALABLE, AND COST-EFFECTIVE RECONFIGURATION, VIRTUALIZATION, AND FAULT-TOLERANCE SUPPORT FOR ON-CHIP NETWORKS



Francisco Triviño García
University of Castilla-La Mancha, Spain
Advisors: Dr. Francisco José Alfaro Cortés and Dr. José Luis Sánchez García
June 2013

Our efforts in this thesis have focused on providing the network-on-chip (NoC) new functionalities such as virtualization, fault-tolerance and reconfiguration support in a fast, efficient, and scalable manner. One remarkable contribution is the development of a virtualization framework based on NoC partitioning in order to achieve traffic isolation. Moreover, this dissertation deals with NoC configuration strategies able to support faults in the NoC. Obviously, a system enabling these new functionalities will continuously change among NoC configurations. We also propose an extremely fast reconfiguration framework that allows the NoC to change the routing function in a deadlock-free manner.

EXPLOITING MULTI-LEVEL PARALLELISM IN STREAMING APPLICATIONS FOR HETEROGENEOUS PLATFORMS WITH GPUS

Ana Balevic
University of Leiden, The Netherlands
Advisors: Prof. Dr. Ed Deprettere and Dr. Bart Kienhuis
June 2013

Modern heterogeneous platforms provide the opportunity to exploit parallelism at different platform levels. However, the diversity of architectures and programming models makes tapping into the platform potential a challenging task. In this thesis, we propose a novel methodology for compile-time generation of structured, multi-level programs (MLPs) from sequential applications. As fundamental contributions, we introduce a novel hierarchical intermediate program representation (HiPRDG) and a method to construct MLPs featuring multiple forms of parallelism (task, data, pipeline), thus opening the door towards efficient, tailor-made parallelization for heterogeneous platforms with accelerators.

DESIGN AND IMPLEMENTATION OF SOFTWARE DEFINED RADIOS ON A HOMOGENEOUS MULTI-PROCESSOR ARCHITECTURE

Roberto Airoldi
Tampere University of Technology, Finland
Advisor: Prof. Jari Nurmi
June 2013

This doctoral thesis deals with issues related to the design of flexible radio platforms. In particular, the research work focuses on the utilization of homogeneous multi-processor (MP) architectures as a feasible way to efficiently implement SDR platforms. In fact, platforms based on MP architectures are able to deliver high performance together with a high degree of flexibility. Moreover, homogeneous MP platforms are able to reduce design and verification costs. HW and SW scalability was identified as the key design parameter to meet the requirements. The proposed architecture and algorithm showed that homogeneous MP architectures are highly scalable platforms, both in terms of HW and SW.

UPCOMING EVENTS

The 9th International Conference on Wireless and Mobile Communications (ICWMC 2013)
21-26 July 2013, Nice, France http://www.iaria.org/conferences2013/ICWMC13.html

The 18th International European Conference on Parallel and Distributed Computing (Euro-Par 2013)
26-30 August 2013, Aachen, Germany http://www.europar2013.org

The 23rd International Conference on Field Programmable Logic and Applications (FPL 2013),
2-4 September 2013, Porto, Portugal, http://www.fpl2013.org

The 22nd International Conference on Parallel Architectures and Compilation Techniques (PACT 2013)
7-11 September 2013, Edinburgh, Scotland http://www.pactconf.org

23th International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS 2013)
9-11 September 2013, Karlsruhe, Germany http://www.itiv.kit.edu/patmos-vari2013

International Conference on Parallel Computing (ParCo 2013)
10-13 September 2013, Munich, Germany http://www.mac.tum.de/parco2013

The 5th Mini-Symposium on Parallel Computing with FPGAs (ParaFPGA 2013)
10-13 September 2013, Munich, Germany http://parafpga.elis.ugent.be

Conference on Design and Architectures for Signal and Image Processing (DASIP 2013),
8-10 October 2013, Cagliari, Italy http://www.ecsi.org/dasip

International Symposium on System-on-Chip 2013 (SoC 2013)
23-24 October 2013, Tampere, Finland http://soc.cs.tut.fi/

The 46th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO-46),
7-11 December 2013, Davis, California, USA http://www.microarch.org/micro46

The 16th Design, Automation and Test in Europe Conference (DATE 2014),
24-28 March 2014, Dresden, Germany http://www.date-conference.com

The International Conference on Compiler Construction (CC 2014)
5-13 April 2014, Grenoble, France http://www.etaps.org

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20-22 JANUARY 2014, VIENNA, AUSTRIA